

Notice of References Cited	Application/Control No. 10/604,059		Applicant(s)/Patent Under Reexamination PEREZ ET AL.	
	Examiner Nghia M. Doan		Art Unit 2825	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,078,085	06-2000	Suzuki, Hajime	257/369
*	B	US-5,369,595	11-1994	Gould et al.	716/17
*	C	US-5,051,917	09-1991	Gould et al.	716/17
*	D	US-4,988,636	01-1991	Masleid et al.	438/129
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Quincke J., Novel test structure for the investigation of the efficiency of guard ring used for I/O latch-up prevention, March 1990, Vol. 3, pages 35-39.
	V	Ker et al., Automatic methodology for placing the guard ring into chip layout to prevent latch-up in CMOS IC's, Sept 2001, Vol. 1, pages 113-116.
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.